# Core-less Switch Architecture

Switch-Less Dragonfly on Wafers: A Scalable Interconnection Architecture based on Wafer-Scale Integration

Programmable switches based on the Protocol Independent Switch Architecture (PISA) have greatly enhanced the flexibility of today"s networks by allowing new packet protocols to be deployed without ...

Motivated by these, we propose a new interconnection architecture called Switch-less Dragonfly on Wafers. By utilizing distributed high-bandwidth networks-on-chip-on-wafer, we build a scalable wafer ...

Rockport Networks on Oct. 26 announced the commercial availability of its new switchless network architecture, optimized to deliver the heightened data performance and scalability necessary for ...

We will introduce these two approaches in reverse-chronological order, starting with the more general, programmable case of P4. We start by considering a bare-metal switch as a whole, where the best ...

This section describes how the reference architecture for campus deployments can be implemented with the Fortinet solution, leveraging the tiered recommendation described in Wired local area network ...

Typically they provide multiple CPUs (Performance CPU, Management CPU) and require multiple cascaded switches to provide sufficient switch ports and redundancy.

This paper discusses the benefits of a coreless architecture, what it looks like, and a low-risk approach to evolving centralized legacy systems into a coreless architecture that supports innovation.

These notes just scratch the surface of the very deep, interesting, and practical area of switch architecture. We emphasize some key concepts that come up frequently in the design of switches ...

Coreless Architecture represents a significant shift in how IT infrastructure can be designed and deployed. By eliminating the dependency on a centralized core, businesses gain greater flexibility, ...

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